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Design of a Data Error Correction System Based on Associative Memory

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Abstract

Digital data in a network must be transferred from one node to another with perfect accuracy. That means the number of ones and they arrangements in the data received must be equal to the data transmitted. For many applications such case is not always achieved and some corrupted in messages are occurred. There are many mechanisms to detect and correct the errors, and the goal of perfect accuracy in a simple design is not achieved yet. A new method is suggested to guarantee 100% accuracy in correct one more bits of the erring messages. The new strategy uses bidirectional associative memory (BAM) to solve the problem, but the structure of BAM itself suffers from an internal error with the read of the data, so a new design is proposed for the BAM to be suitable for the system. The obtained results from the test examples proved that the proposed method can reach the goal with simple design for the system.

Key words: Error correction; data transmission; artificial neural network; BAM.

1. Introduction

In information theory and coding theory and some remote data communication applications, detect and correct errors or control errors are the technologies that enable reliable connectivity for digital data instead of the unreliable communication channels. These technologies are exclusively applied on digital networks without analogue networks, and for this reason, the digital networks replaces the analogue networks.

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A lot of communication channels are exposed to the noise, which may cause errors during data transmission from the source to the receiver. Error detection techniques help to detect these errors, while correction techniques contribute to re-create the original data. The general idea of the classical correcting processes is to use some additional data to the message - and through which the receiver can stand on the consistency of the received message - and restore data that distorted. There were several mechanisms for detect and correct error, these mechanisms are spirited so many techniques occur to decreasing the bit-errors effect and attempting to guarantee that the receiver not has error version of the packet, one of these mechanisms is Forward error correction (FEC) mechanism, It is a process that can transmit error correction data forever with the message. It is utilized also where there is no backward channel occurs from the receiver to the sender [1]. Block codes and convolutional codes are two main types of codes. Block Code includes constant length vectors known as code words. In implementation term, the block codes are very hard to implement because when its length arises it become very complex. There are two widely utilized examples of block codes named Hamming Codes and Cyclic Redundancy Checks [2]. The hamming Codes able to detect and correct error in a single bit of information block and each bit in these codes is contained in a singular collection of parity bits. If the parities have faults due to a single bit error, it can be found the wrong information bit by adding the positions of the wrong parities. Although these codes implementations are simple, but it had a trouble increases when there is more than one wrong bit in the received message. While cyclic redundancy checks (CRC) is a code word. In the transmitter side, it can utilize a function to determine the CRC check bits value depending on the transmitted information. These CRC bits with the data are sent forever with the receiver. The same computation can perform by the receiver on the received information and contrasts it with the CRC bits that it received. The convolutional Codes created consecutively because through a linear finite-state shift register it crossing the data in consecutive form. Encoding operation is able to produce encoded bits as soon as a little bits have been processed and after that continuous to produce more bits as wanted. In the same way, decoding operation able to begin as soon as received a little bits [3]. Automatic Repeat Request (ARQ) is another mechanism can detect and correct errors, in which if no faults are discovered in the received message the receiver transmits back a positive acknowledgement. But, CRC is determined again by utilizing the received bits at the receiver. This process has many obstacles. Firstly, when the entire message is transmitting, it takes time much larger than the sender when it waiting acknowledgements from the receiver. Secondly, it is not probable to have, two-way communications, real-time, practical due to this delay [4]. While Hybrid Automatic Repeat Request (H-**ARO**) is other type of ARO process. In which error correction data is sent forever with the code. H-ARO includes two variant types, namely Type I HARQ and Type II HARQ. Type I is identical to ARQ unless that in this state before send process the error detection and forward error correction (FEC) bits are appended to the data. In Type II, the first sending is sent with error detection data only. While the second sending is sent forever with error correction data if this sending is not received error free. The data from these two packets able to collected to remove the error [5]. Viterbi Mechanism is the perfect error correction process utilized actually in systems of communication. It is tradeoff between power consumption and complexity of hardware [6]. The Viterbi decoding may be executed by two major mechanisms called, Register Exchange mechanism and Traceback mechanism. The first mechanism can save the partly decoded output sequence forever the path. At every stage, the contents of every register must copy to the next stage. This thing makes the hardware more energy consumption and complex than the second mechanism. The second mechanism utilizes a singular bit to mention whether the survivor department came from the upper or the lower way. This mechanism demonstrates to be less energy consumption [7].

1.1 Bidirectional Associative Memories

In general, the associative memory is a neural network connecting points of input side with the points of the output side in a manner so as to ensure each output has a corresponding input [8], all the interconnection information are stored as a weight matrix [M] as shown in Figure(1),

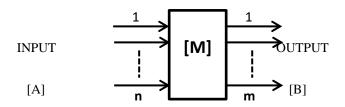


Figure 1: General structure of the associative memory

Where A and B are the input and output vectors respectively, n and m are the word-length of A and B respectively, and i is the number of A:B patterns.

Determination of the connection weight matrix [M] is known as encoding [9], and it is given by: $M = \sum_i A_i^T B_i$

While recall B_i or A_i are achieved by decoding process depending on:

$$B_i = A_i M \tag{2}$$

And

$$A_i = B_i M^T \tag{3}$$

Associative memory can be hetero-associative in which the information of input and output data are different, or auto-associative where the input/output vectors are similar, ie [B] = [A]. Bidirectional associative memory (BAM) is hetero-associative memory, it has the ability of reading data from input or output side, by other words, [A] is considered the input to the system and [B] is output or vice versa. In addition, BAM has the ability of correcting errors by applying the data many times through the network in both directions [10]. The use of BAM in many applications is very limited because of two matters: the low storage capacity of the memory (maximum number of pattern pairs that can be stored is not exceed the word length of A and B), and the error problem often be occurred with extracting output data [11].

2. Materials and methods

2.1 The Proposed Strategy for Error correction Process

Using the BAM to achieve perfect error correction technique in very simple way is the goal of the new strategy. Before that, the performance of the BAM must be improved to overcome the two main drawbacks of the reading error data and low storage capacity. So a new algorithm is optimized to solve these problems.

Figure (2) illustrate the new encoding process. The factor (S) is the summation of (B) bits, and (P) is the power function which is given by:

$$P = A \times M \tag{4}$$

While the energy function value (E) is given by:

$$E = A \ M \ B^T \tag{5}$$

The obtained P and E values have not to be zero, otherwise B must be regenerated until disappear all the zeros.

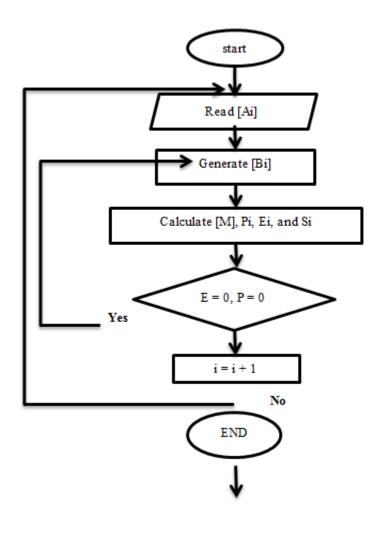


Figure 2: Encoding part of the error correction procedure

In the decoding of A, the error detection and correction will be achieved. The procedure is given in figure (3). It is initially started supposing default value for B vector with all elements equal to unity, then the energy function, power function, summation factor, as well as the deference between the main energy function and the calculated energy function (Di) are determined. The contents of the B vector are changed bit by bit and at each step the value of Di must be reduced approaching to zero, and if not, the bit have not to be changed. When the entire calculated parameters equal to the encoding parameters, the procedure is finished with the correct value of Bi and then its corresponding Ai and any error bit will be corrected.

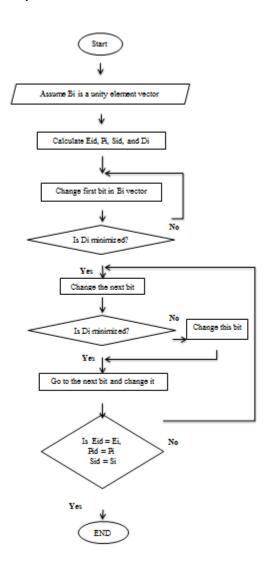


Figure 3: Decoding part of the error correction procedure

3. Results

3.1 Test Example

Consider the four pattern pairs (A1, B1), (A2,B2), (A3,B3), (A4,B4) given by:

 $A1 = [1 \ 0 \ 1 \ 0] \qquad B1 = [1 \ 0 \ 1]$

A2 = [0 1 0 1]	B2 = [0 1 0]
A3 = [0 0 1 1]	B3 = [1 1 0]
A4 = [0 0 0 1]	B4 = [0 0 1]

In bipolar form, the patterns will be:

X1 = [1-11-1]	Y1 =[1-11]
X2 = [-1 1 -1 1]	Y2 = [-1 1 -1]
X3 = [-1 -1 1 1]	Y3 = [1 1 -1]
X4 = [-1 -1 -1 1]	Y4 = [-1 -1 1]

Encoding process:

Calculate M from equation (1).

$$\mathbf{M} = \left[\begin{array}{cccc} 2 & -2 & 2 \\ -2 & 2 & -2 \\ 4 & 0 & 0 \\ -2 & 2 & -2 \end{array} \right]$$

Calculating pi from equation (4) gives:

p1= [10 -6 6], p2= [-10 6 -6], p3= [2 2 -2], p4= [-6 2 -2]

and Ei from equation (5) gives:

E1= 22, E2= 22, E3=6, E4=2

Calculate the summation for each (Y) pattern (Si)

s1=1, s2=-1, s3=1, s4=-1

Decoding process:

To recall Y1, let B1= [1 1 1], E1=22, S1= 1

- E1d = 10 < 22 (main value), S1d=3, D1=12
- E1d = -10 error (go away from 10), S1d=1, D1=32
- E1d = 22 = E1, and s1d=1 = S1, D1=0, so Y1=[1 1 1]
- To recall Y2, let B2=[1 1 1], E2 =22, S2 = -1
- E2d = -10 < 22 (main value), S2d=3, D2=32
- E2d = 10 < 22 (approach from 22), S2d=1, D2=12
- E2d = -2 error (go away from 22), S2d = -1, D2 = 24
- E2d = 22 = E2, and s2d = -1 = S2, D2 = 0, so $Y2 = [-1 \ 1 \ -1]$
- To recall Y3, let B3= [111], E3 =6, S3 = 1
- E3d = 2 < 6 (main value), S3d=3, D3=4
- $E3d = -2 \operatorname{error} (\operatorname{go} \operatorname{away} \operatorname{from} 6), S3d=1, D3=8$
- E3d = -2 error (stay on the same value, i.e -2), S3d=1, D3=8
- E3d = 6 = E3, and S3d=1 = S3, D3=0, so $Y3=[1 \ 1 \ -1]$
- To recall Y4, let B4= [1 1 1], E4 =2, S4 = -1
- E4d = -6 < 2 (main value), S4d=3, D4=8
- E4d = 6 big error (cross the main value, i.e 2), S4d=1, D4=4
- E4d = -10 error (go away from 2), S4d=1, D4=12

E4d = -2 (approach from 2) in this case it reach to the last bit of supposed B4, but the two conditions not satisfied, it must repeat the algorithm above on the final result from beginning, S4d=1, D4=4

$$E4d = [-6 \ 2 \ -2] \begin{pmatrix} -1 \\ 1 \\ -1 \end{pmatrix} = 10 > 2, \ S4d = -1, \ D4 = 8$$

$$E4d = \begin{bmatrix} -6 & 2 & -2 \end{bmatrix} \begin{pmatrix} -1 \\ -1 \\ -1 \end{pmatrix} = 6 > 2 \text{ (approaching from 2), S4d} = -3, D4 = 4$$
$$E4d = \begin{bmatrix} -6 & 2 & -2 \end{bmatrix} \begin{pmatrix} -1 \\ -1 \\ 1 \\ 1 \end{pmatrix} = 2 = E4, \text{ and S4d} = -1 = S4, D4 = 0, \text{ so Y4} = \begin{bmatrix} -1 & -1 & 1 \end{bmatrix}$$

The solved example proves the efficiency of the new method is 100% in prediction of the associated pair (Bi), and thus the data information of the received word (Ai). Figure (4) demonstrates how the new method works with an image example of a letter N. it is clear that the system has the full ability to correct the errors regardless of the number of error bits.

1	-1	-1	-1	-1	1
1	1	-1	-1	-1	1
1	-1	1	-1	-1	1
1	-1	-1	1	-1	1
1	-1	-1	-1	1	1
1	-1	-1	-1	-1	1

1	-1	-1	1	-1	1
-1	1	1	-1	1	-1
1	-1	1	-1	-1	1
1	-1	-1	1	-1	1
1	-1	-1	-1	1	1
1	-1	-1	-1	-1	1

A: (X) patterns values

B: Decoding (X) patterns with errors

1	-1	-1	-1	-1	1
1	1		-1	-1	1
1	-1	1	-1	-1	1
1	-1	-1	1	-1	1
1	-1	-1	-1	1	1
1	-1	-1	-1	-1	1

C: Decoding (X) patterns after correct error

Figure 4: Error correction in letter N

4. Conclusion

A new method has been developed to be used in error detection and correction systems taking advantage of the bidirectional associative memory. The encoding and decoding of the BAM has also been developed to be efficient and without defects.

The tests validate the new method and proved its ability to correct errors regardless the number of error bits. It achieves 100% efficiency in the process.

The new design provides a simple structure for the system. It has also the ability of converting the data to another form with a less word length which makes the BAM very useful in memory applications.

References

- J. Ababneh, O. Almomani, "Survey of Error Correction Mechanisms for Video Streaming over the Internet", International Journal of Advanced Computer Science and Applications, Vol. 5, No. 3, 2014.
- [2] V. Gupta, Ch. Verma, "Error Detection and Correction: An Introduction", International Journal of Advanced Research in Computer Science and Software Engineering, vol.2, iss.11, nov.2012.
- [3] D. Mishra, T.V.S Ram, K S Dasgupta, and S.Jit, "Concatenated Convolutional Codes for Deep Space Mission", International Journal of Information and Communication Technology Research, vol.2, no.6, jun.2012.
- [4] Y. Bulo , M. Anju , Ch. T Bhunia , "ARQ Technique with Aggressive Packet Combining Scheme for Variable Error Rate Channels to Reduce the Bandwidth and Power Consumption", International Journal of Applied Engineering Research, Vol. 11, No. 5 , 2016.
- [5] U. Datta , D. B. Kumar, A. K. Ball , S. Kundu, "Performance of a Hybrid ARQ Scheme in CDMA Wireless Sensor Network", International Journal of Energy, Information and Communications , Vol. 2, Iss. 3, Aug. 2011.
- [6] V. P. Patil, Prof. D. G. Chougule, R..R.Naik, "Viterbi Algorithm for error detection and correction", IOSR Journal of Electronicsl and Communication Engineering (IOSR-JECE), ISSN: 2278-2834-, ISBN: 2278-8735.
- [7] C. ARUN, V. RAJAMANI, "A Low Power and High Speed Viterbi Decoder Based on Deep Pipelined, Clock Blocking and Hazards Filtering", Int. J. Communications, Network and System Sciences, 2009.
- [8] B.D.C.N.Prasad, P E S N Krishna Prasad, S. Yeruva, and P Sita Rama Murty, " A Study on Associative Neural Memories", International Journal of Advanced Computer Science and Applications (IJACSA), Vol. 1, No. 6, Dec. 2010.

- [9] A. Damara, V. Damara, A. Chanana, "Associative Memory: A Memory", International Journal of Innovative Research in Engineering & Science, issue 2 volume 10, October 2013.
- [10] B. Kosko, "Adaptive bidirectional associative memories", Applied Optics Journal, Vol. 26, No. 23, Dec. 1987.
- [11] N. Abd Alhadi Jabr, and E. I Abdul Kareem, "Modify Bidirectional Associative Memory (MBAM)", International Journal of Modern Trends in Engineering and Research (IJMTER) ,Vol. 02, Iss.08, Aug. 2015.